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# Specification

## COG-BT96040A-03

### Doc. No.: VL-FS-COG-BT96040A-03 REV.A

**Version March 2007**

**DOCUMENT REVISION HISTORY**

| DOCUMENT REVISION FROM TO | DATE | DESCRIPTION | CHANGED BY | CHECKED BY |
|---|---|---|---|---|
| A | 2007.03.23 | First Release.<br>Based on<br>a.) Test Specification:<br>VL-TS-COG-BT96040A-XX REV.A 2007.02.08<br>b.) VL-QUA-012B REV.W 2004.03.20<br><br>According to VL-QUA-012B, LCD size is small because Unit Per Laminate=28 which is more than 6pcs/Laminate. | LINDA ZHU | VIVIAN LUO |

# CONTENTS

**Specification**
**of**
**LCD Module Type**
**Item No.: COG-BT96040A-03**

## 1. General Description

- 96 x 40 dots STN Yellow Positive Reflective Dot Matrix LCD module.
- Viewing angle: 12 O'clock.
- Driving scheme: 1/49 duty, 1/8 bias.
- Driving IC: 'ST' STE2004S (COG form) LCD controller/driver or equivalent.
- Logic voltage: 3V.
- "RoHS" compliance.

## 2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

| Parameter | Specifications | Unit |
|---|---|---|
| Outline dimensions | 46.0(W) x 36.2(H) x 1.98(D) (Excluded pins and EPOXY) | mm |
| Viewing area | 40.0(W) x 23.0(H) | mm |
| Active area | 35.217(W) x 18.225(H) | mm |
| Display format | 96 x 40 | dots |
| Dot size | 0.352(W) x 0.441(H) | mm |
| Dot spacing | 0.015(W) x 0.015(H) | mm |
| Dot pitch | 0.367 (W) x 0.456(H) | mm |
| Weight: | Approx: 6.5 | gram |

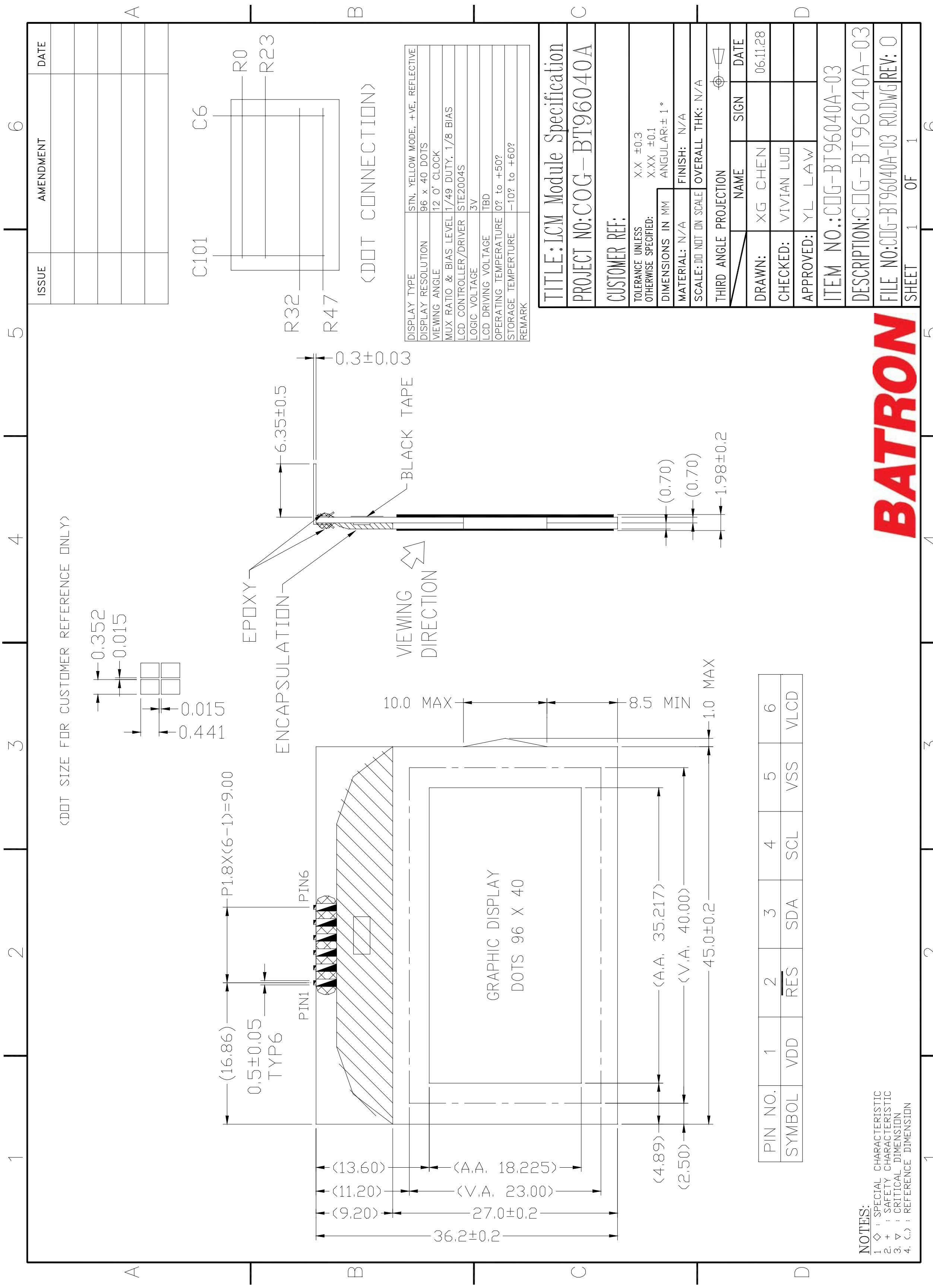



Figure 1: Module Specification

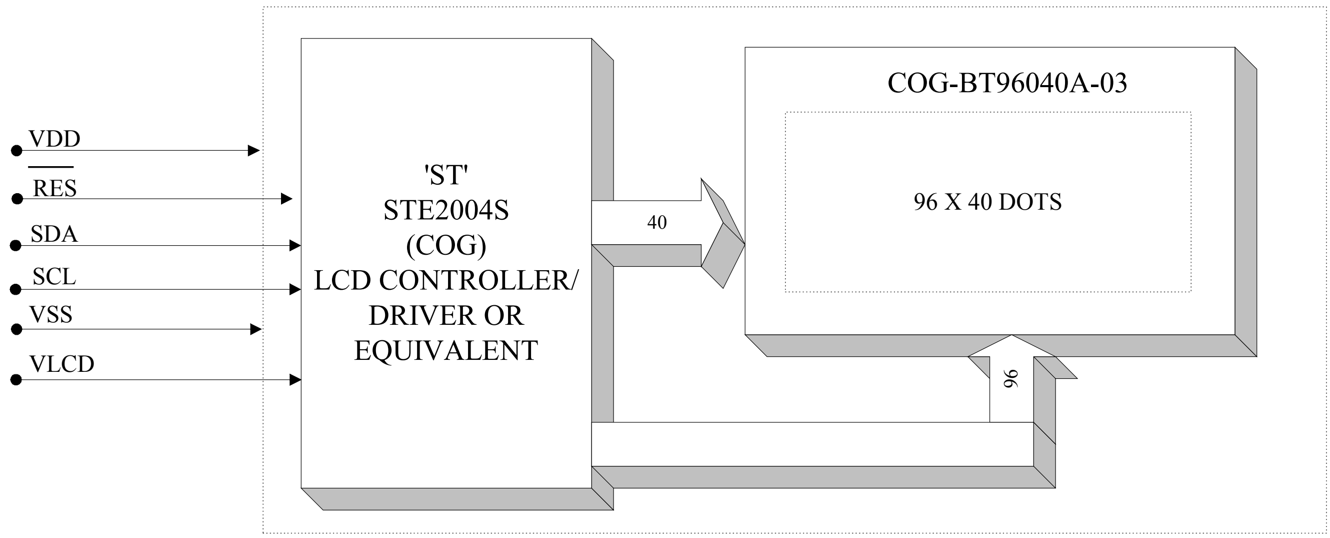



Figure 2: Block Diagram

## 3. Interface signals

Table 2

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | VDD | Power supply for logic (+3V). |
| 2 | $\overline{RES}$ | Reset Input. Active Low. |
| 3 | SDA | $I^2C$ Bus Data Out IF UNUSED MUST BE LEFT FLOATING. |
| 4 | SCL | $I^2C$ bus Clock - CANNOT BE LEFT FLOATING. |
| 5 | VSS | Ground (0V). |
| 6 | VLCD | Power supply for LCD driver. |

# 4. Absolute Maximum Ratings

## 4.1 Electrical Maximum Ratings-For IC Only

Table 3

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Power Supply voltage | VDD(=VDD1=VDD2) | -0.5 | +5.0 | V |
| Input voltage (all input pads) | Vin | -0.5 | VDD1+0.5 | V |
| Power Supply voltage (LCD drive) | VLCD | -0.5 | +15.0 | V |

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

## 4.2 Environmental Condition

Table 4

| Item | Operating Temperature (Topr) | | Storage Temperature (Tstg) (Note 1) | | Remark |
|---|---|---|---|---|---|
| | Min. | Max. | Min. | Max. | |
| Ambient Temperature | 0°C | +50°C | -10°C | +60°C | Dry |
| Humidity (Note 1) | 90% max. RH for Ta ≤ 40°C<br><50%RH for 40°C <Ta≤ Maximum operating temperature | | | | No condensation |
| Vibration (IEC 68-2-6)<br>cells must be mounted on a suitable connector | Frequency: 10 ~ 55 Hz<br>Amplitude: 0.75 mm<br>Duration: 20 cycles in each direction. | | | | 3 directions |
| Shock (IEC 68-2-27)<br>Half-sine pulse shape | Pulse duration: 11 ms<br>Peak acceleration: 981 $m/s^2$ = 100g<br>Number of shocks: 3 shocks in 3 mutually perpendicular axes. | | | | 3 directions |

Note 1: Product cannot sustain at extreme storage conditions for long time.

## 5. Electrical Specifications

### 5.1 Typical Electrical Characteristics

**At Ta = 25 °C, VDD =VDD1=VDD2= +3.0V±5%, VSS=0V.**

Table 5

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage (Logic) | VDD-VSS | | 2.85 | 3.0 | 3.1 5 | V |
| Supply voltage (LCD) (built-in) | VLCD-VSS | Ta=0 °C, VDD =3V, Note 1 | 9.71 | 10.22 | 10.73 | V |
| | | Ta=+25 °C, VDD =3V, Note 1 | 9.63 | 10.11 | 10.58 | V |
| | | Ta=+50 °C, VDD =3V, Note 1 | 9.35 | 9.85 | 10.34 | V |
| Logic HIGH Voltage Level | $V_{IH}$ | | 0.7 VDD1 | - | VDD2 | V |
| Logic LOW voltage level | $V_{IL}$ | | VSS | - | 0.3 VDD1 | V |
| Supply Current (Logic & LCD) | IDD | Note 1, VDD = 3V, Character mode | - | 0.3 | 0.45 | mA |
| | | Note 1, VDD = 3V, Checker board mode | - | 0.5 | 0.75 | mA |

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

## 5.2 Timing Specifications

**Reset Timing**

**Ta = 0 °C to +50 °C, VDD =VDD1=VDD2= +3.0V±5%, VSS=0V;**

Table 6

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **INTERNAL OSCILLATOR** | | | | | | |
| $F_{OSC}$ | Internal Oscillator frequency | $V_{DD}$ = 2.8V; Tamb = -20 to +70 °C | 61 | 72 | 83 | kHz |
| $F_{EXT}$ | External Oscillator frequency | | 20 | | 100 | kHz |
| $F_{FRAME}$ | Frame frequency | fosc or fext = 72 kHz; note 1 | | 75 | | Hz |
| $T_{W(RES)}$ | RES LOW pulse width | | 5 | | | µs |
| | Reset Pulse Rejection | | | | 1 | µs |
| $T_{LOGIC}$ (RES) | Internal Logic Reset Time | | | | 5 | µs |
| $T_{VDD}$ | VDD1 vs. VDD2 Delay | | 0 | | | µs |

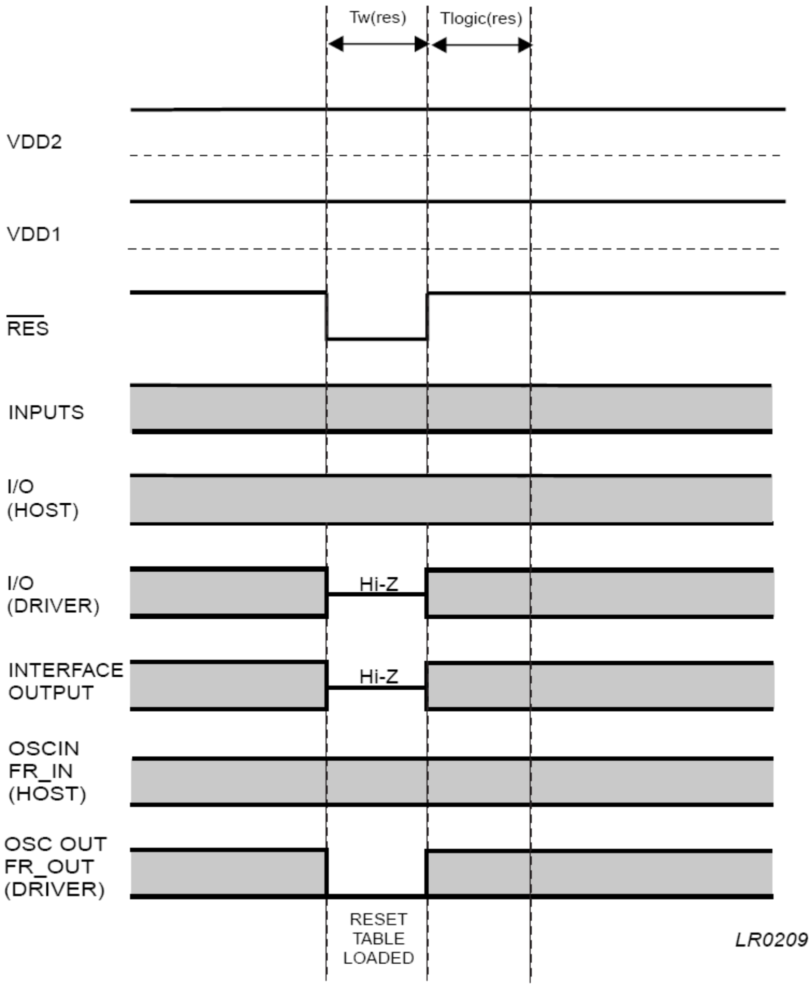



Figure 3: Reset Timing Diagram

**$I^2C$ BUS INTERFACE**

**Ta = 0 °C to +50 °C, VDD =VDD1=VDD2= +3.0V±5%, VSS=0V;**

Table 7

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **$I^2C$ BUS INTERFACE** (See note 4, 7) | | | | | | |
| $F_{SCL}$ | SCL Clock Frequency | Fast Mode | DC | | 400 | kHz |
| | | High Speed Mode; Cb=100pF (max);note 6;VDD1=2 | DC | | 3.4 | MHz |
| | | High Speed Mode; Cb=400pF (max);note 6; VDD1=2 | DC | | 1.7 | MHz |
| | | Fast Mode; note 6; VDD1=1.7V | | | 400 | KHz |
| $T_{SU;STA}$ | Set-up time (repeated) START Condition | Note 2,3, Cb = 100pF | 160 | | | ns |
| $T_{HD;STA}$ | Hold Time (repeated) START Condition | Note 2,3, Cb = 100pF | 160 | | | ns |
| $T_{LOW}$ | Low Period of SCLH Clock | Note 2,3, Cb = 100pF | 160 | | | ns |
| $T_{HIGH}$ | HIGH Period of SCLH Clock | Note 2,3, Cb = 100pF | 160 | | | ns |
| $T_{SU;DAT}$ | Data set-up Time | Note 2,3, Cb = 100pF | 60 | | | ns |
| $T_{HD;DAT}$ | Data Hold Time | Note 2,3, Cb = 100pF | 10 | | | ns |
| $T_{r;CL}$ | Rise Time of SCLH Signal | Note 2,3, Cb = 100pF | 10 | | | ns |
| $T_{r;CL1}$ | Rise Time of SCLH Signal after a repeated START condition and aftyer an Acknowledge bit | Note 2,3, Cb = 100pF | 10 | | | ns |
| $T_{f;CL}$ | Fall time of SCLH signal | Note 2,3, Cb = 100pF | 10 | | | ns |
| $T_{r;DA}$ | Rise time of SCLH signal | Note 2,3, Cb = 100pF | 10 | | | ns |
| $T_{f;DA}$ | Fall time of SDAH signal | Note 2,3, Cb = 100pF | 10 | | 80 | ns |
| $T_{r;DA}$ | Rise Time of SDAH signal | Note 2,3, Cb = 400pF | 20 | | | ns |
| $T_{f;DA}$ | Fall Time of SDAH signal | Note 2,3, Cb = 400pF | 20 | | 160 | ns |
| $T_{SU;STO}$ | Setup Time for STOP condition | Note 2,3, Cb = 100pF | 160 | | | ns |
| Cb | Capacitive Load for SDAH and SCLH | | 100 | | 400 | pF |
| Cb | Capacitive Load for SDAH +SDA line and SCLH +SCL Line | | | | 400 | pF |

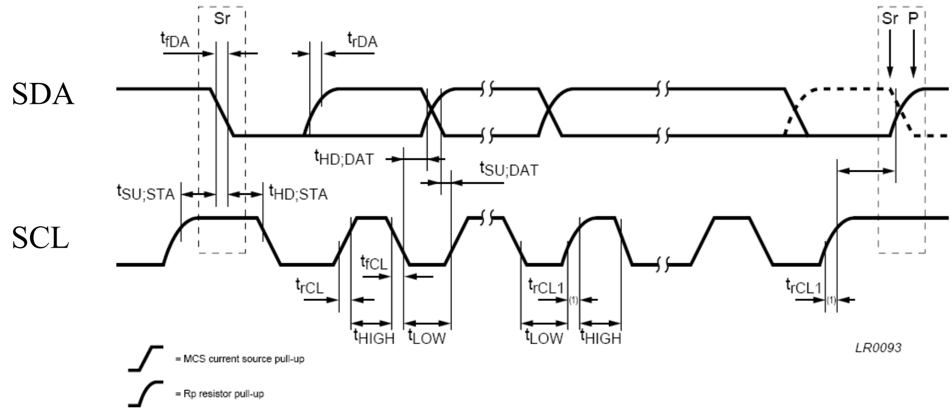


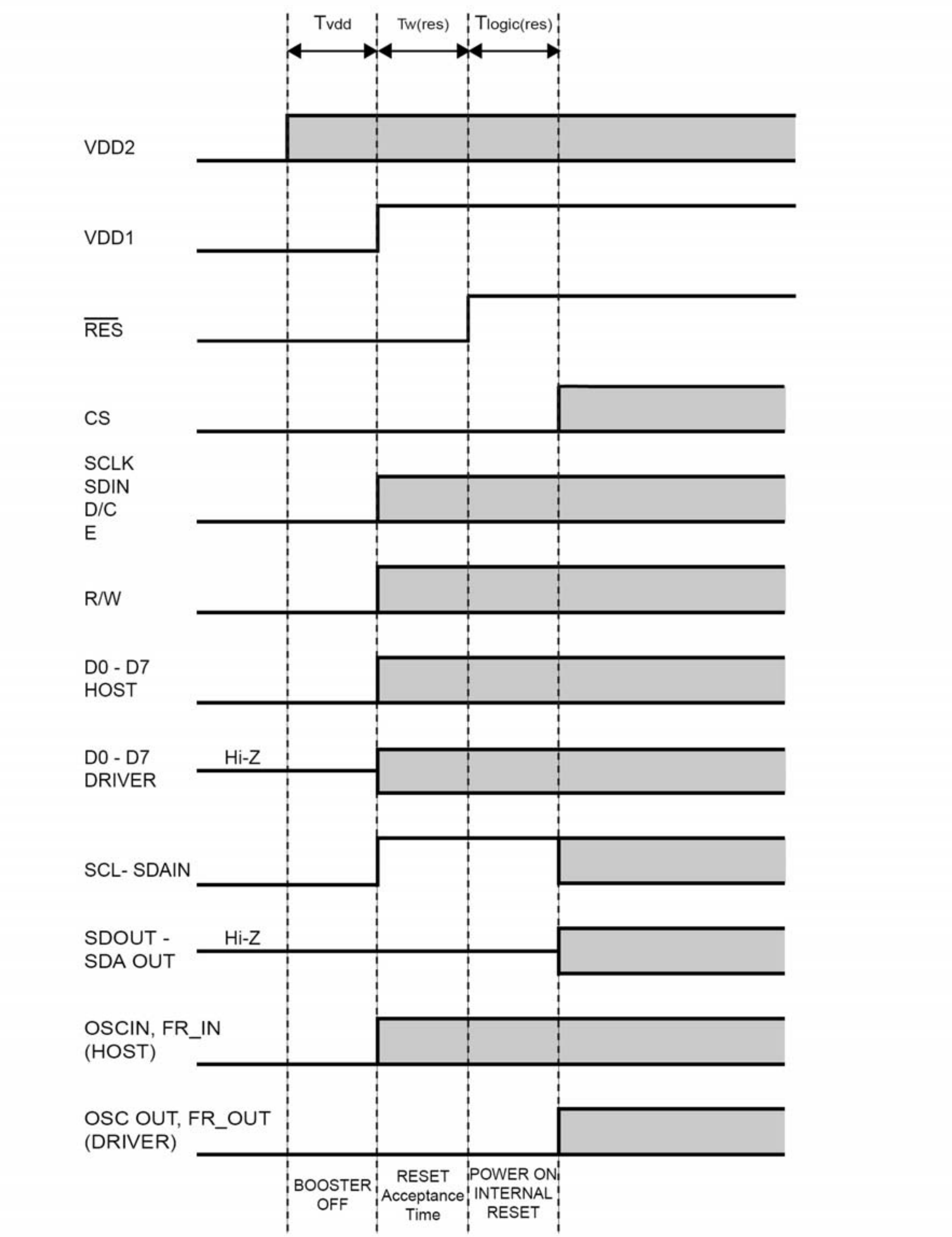

Figure 4: $I^2C$ bus timing diagram

Notes: 1. $F_{frame} = \frac{f_{osc}}{960}$

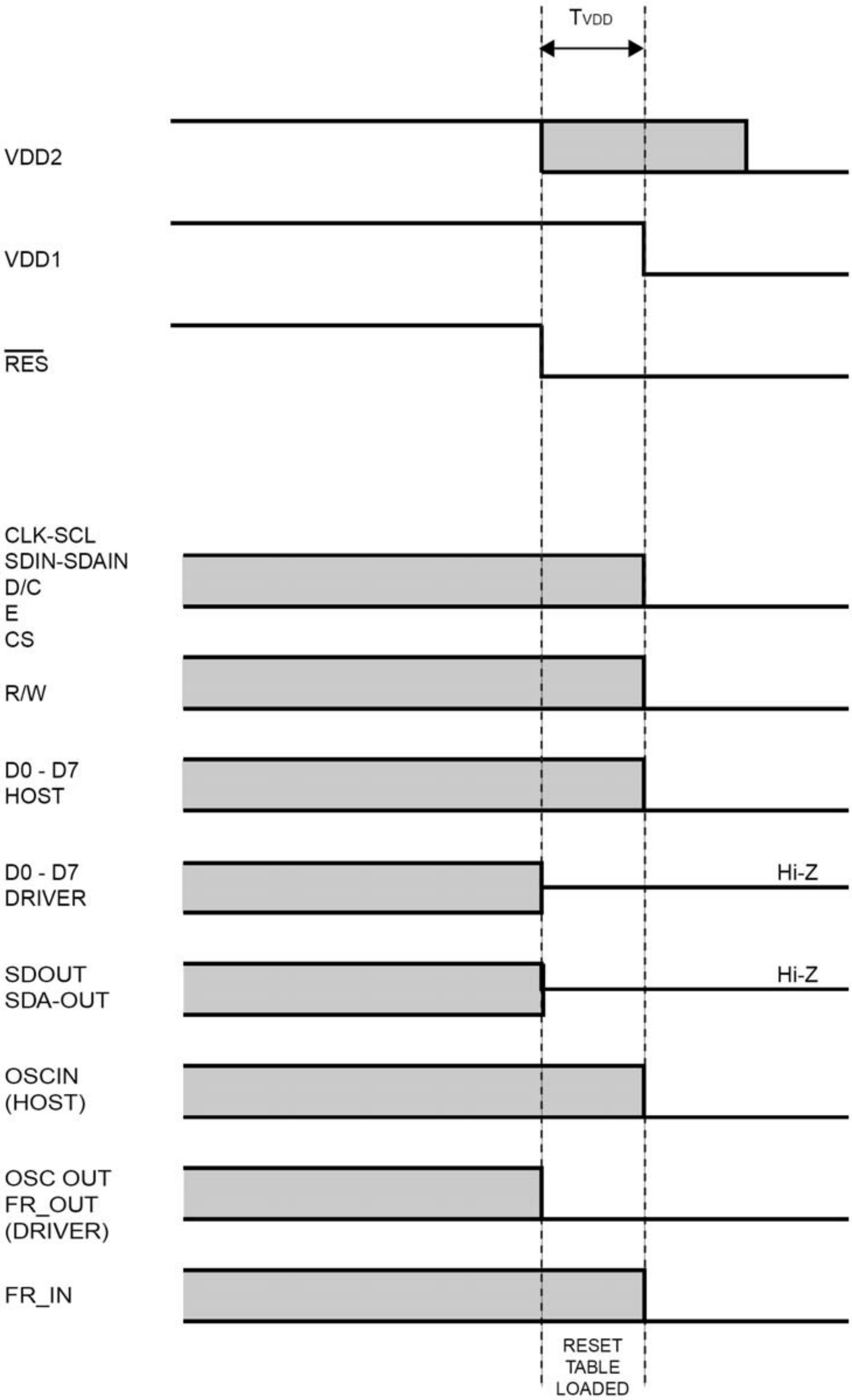
2. All timing values are valid within the operating supply voltage and ambient temperature ranges and referenced to $V_{IL}$ and $V_{IH}$ with an input voltage swing of $V_{SS}$ to $V_{DD}$.
3. Cb is the capacitive load for each bus line.
4. For bus line loads Cb between 100 and 400pF the timing parameters must be linearly interpolated
5. $C_{VLCD}$ is the filtering CApacitor on VLCD
6. Trise and Tfall (30%-70%) -10ns
7. $I^2C$ bus AC Characteristics are tested by correlation

### 5.3 Power on/off timing diagram

**1) Power on timing diagram**



**2) Power off timing diagram**



## 6. LCD Specifications

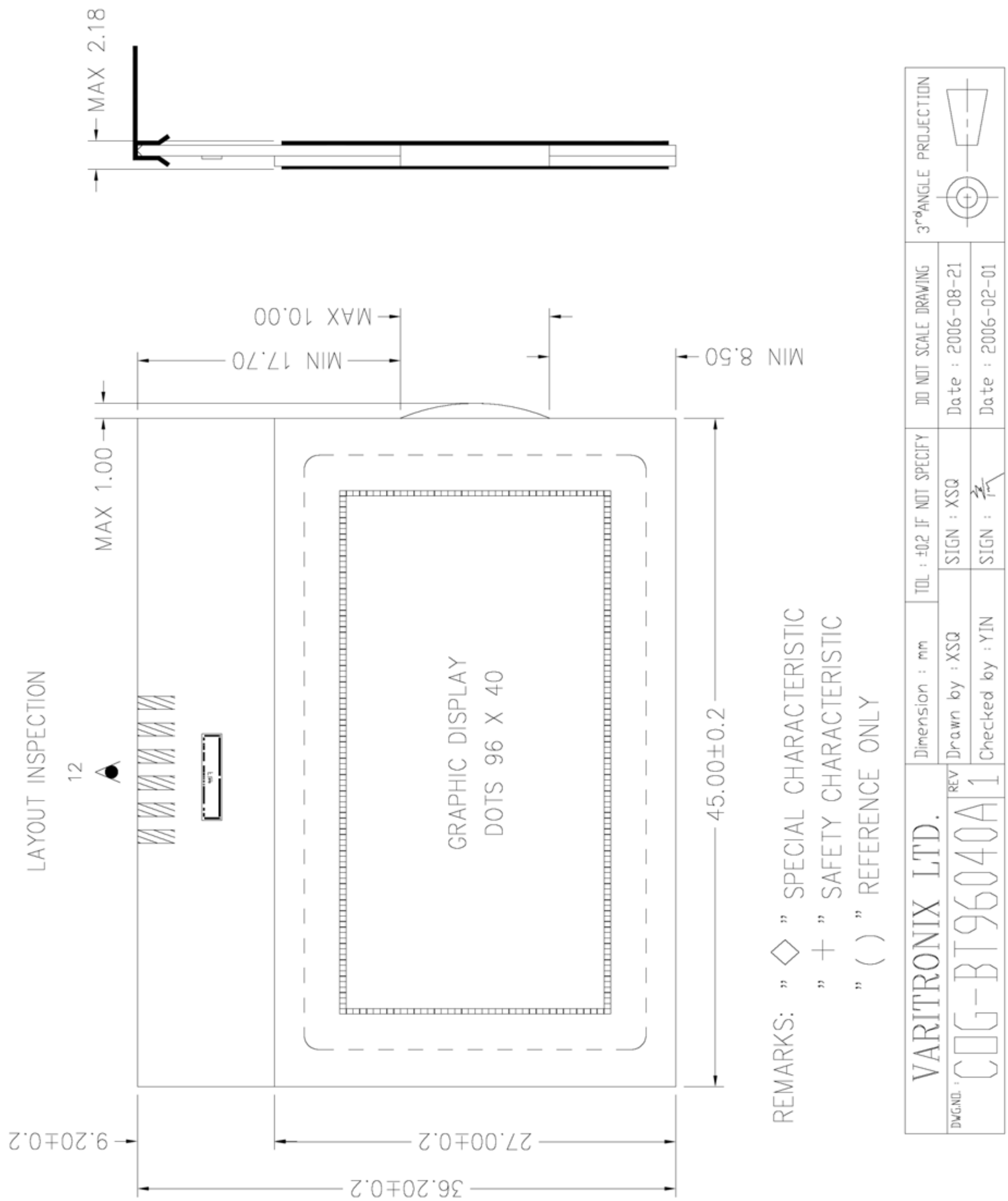



Figure 5: LCD drawing 1

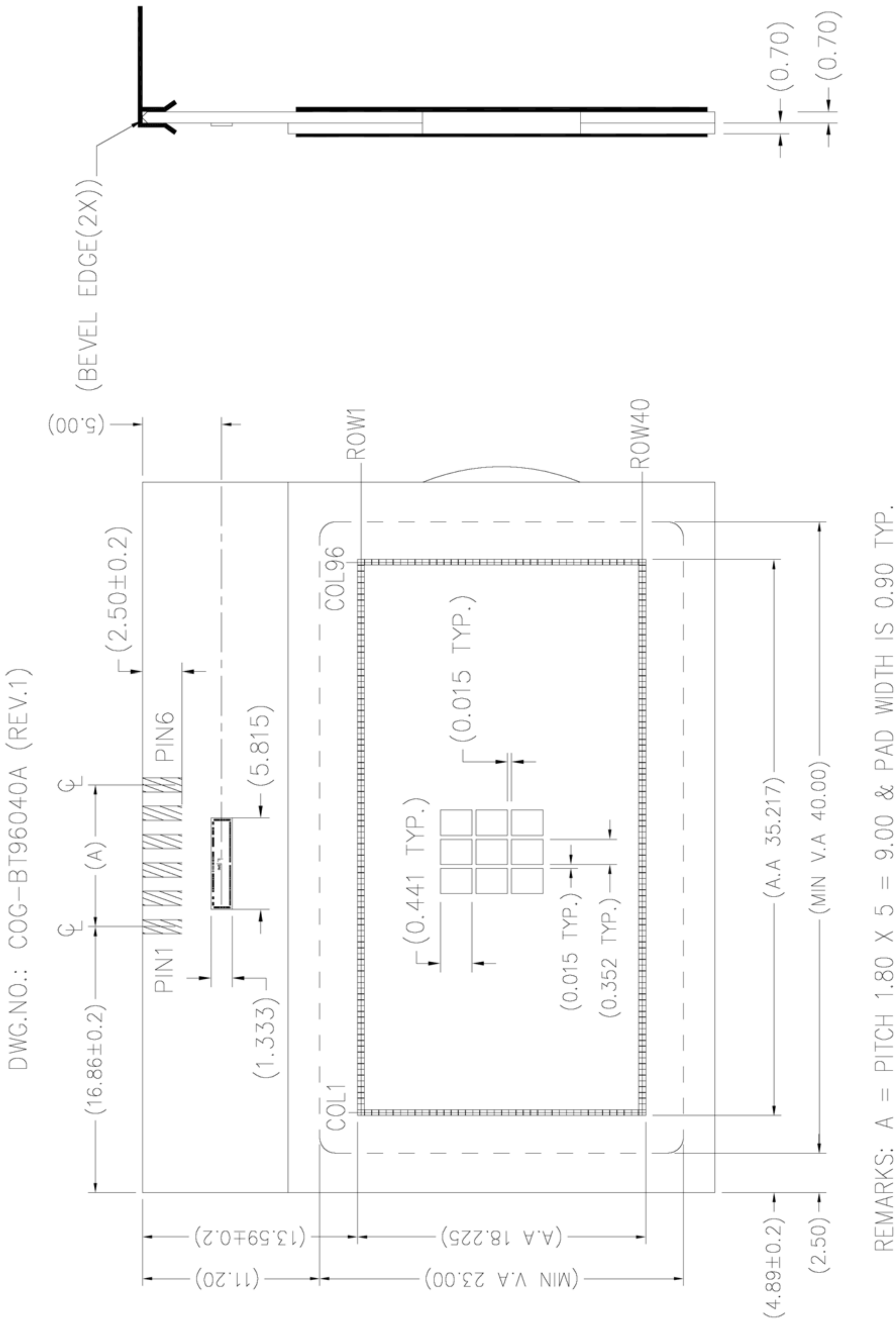



Figure 6: LCD drawing 2

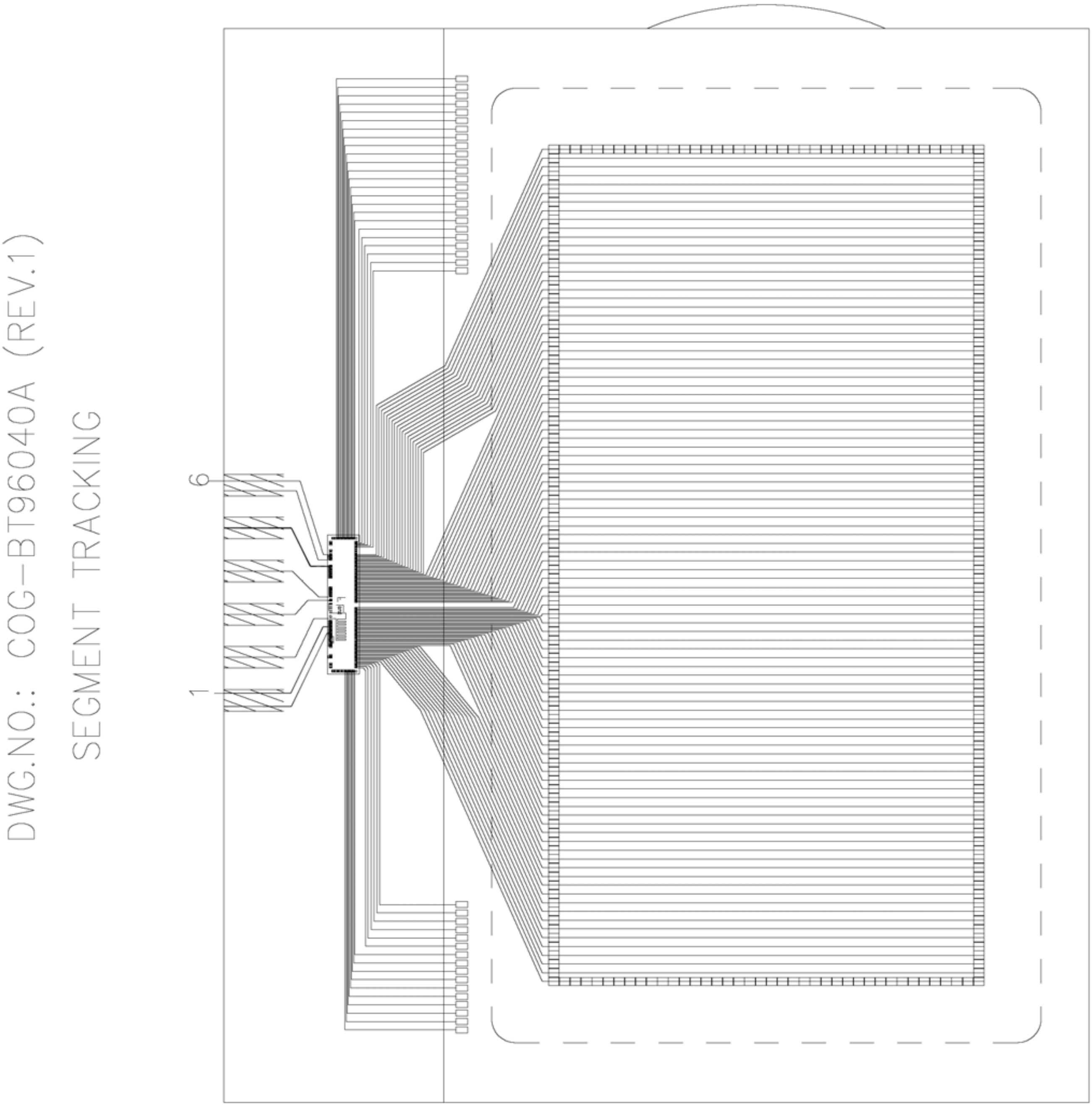



Figure 7: LCD drawing 3

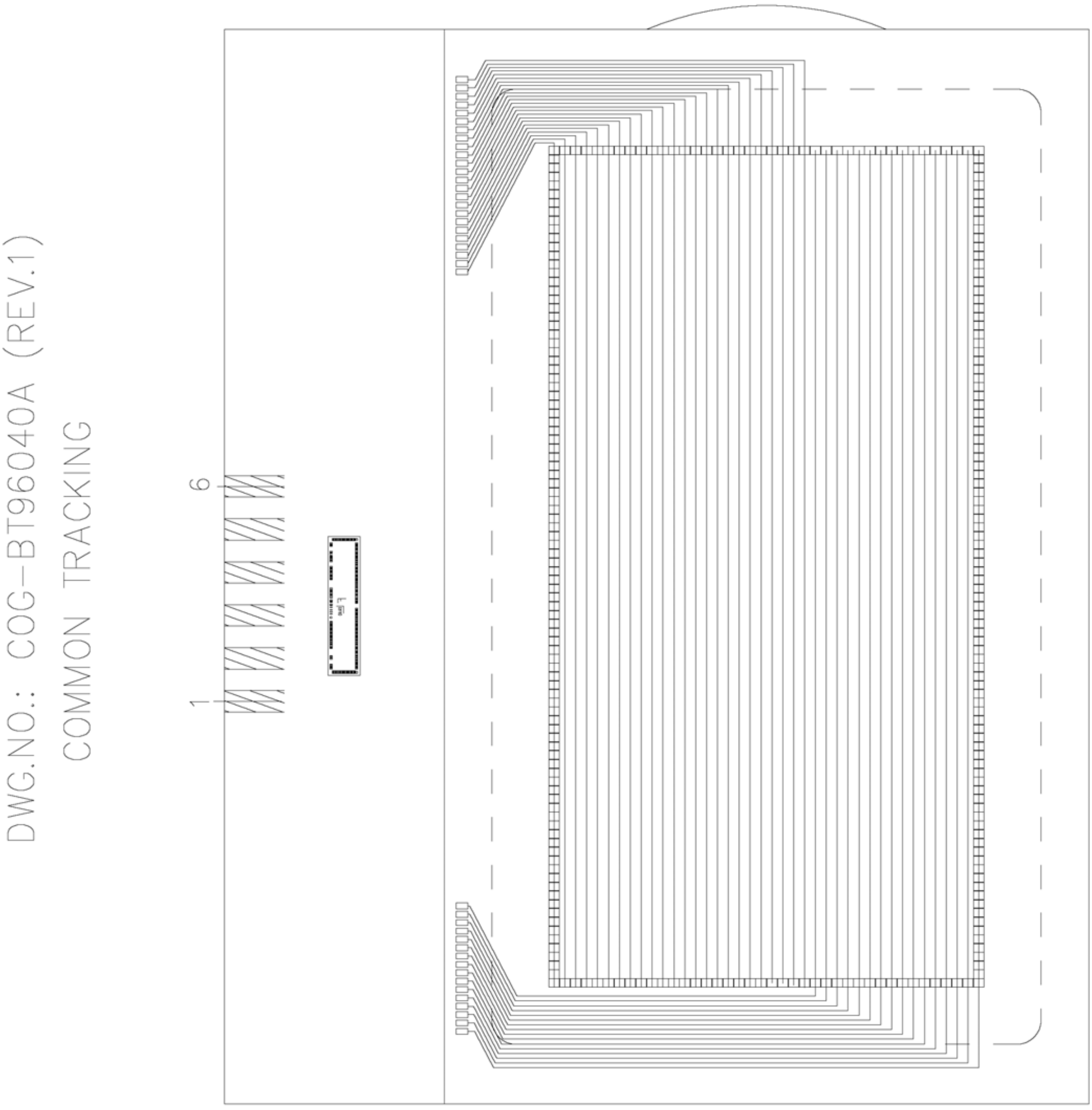



Figure 8: LCD drawing 4

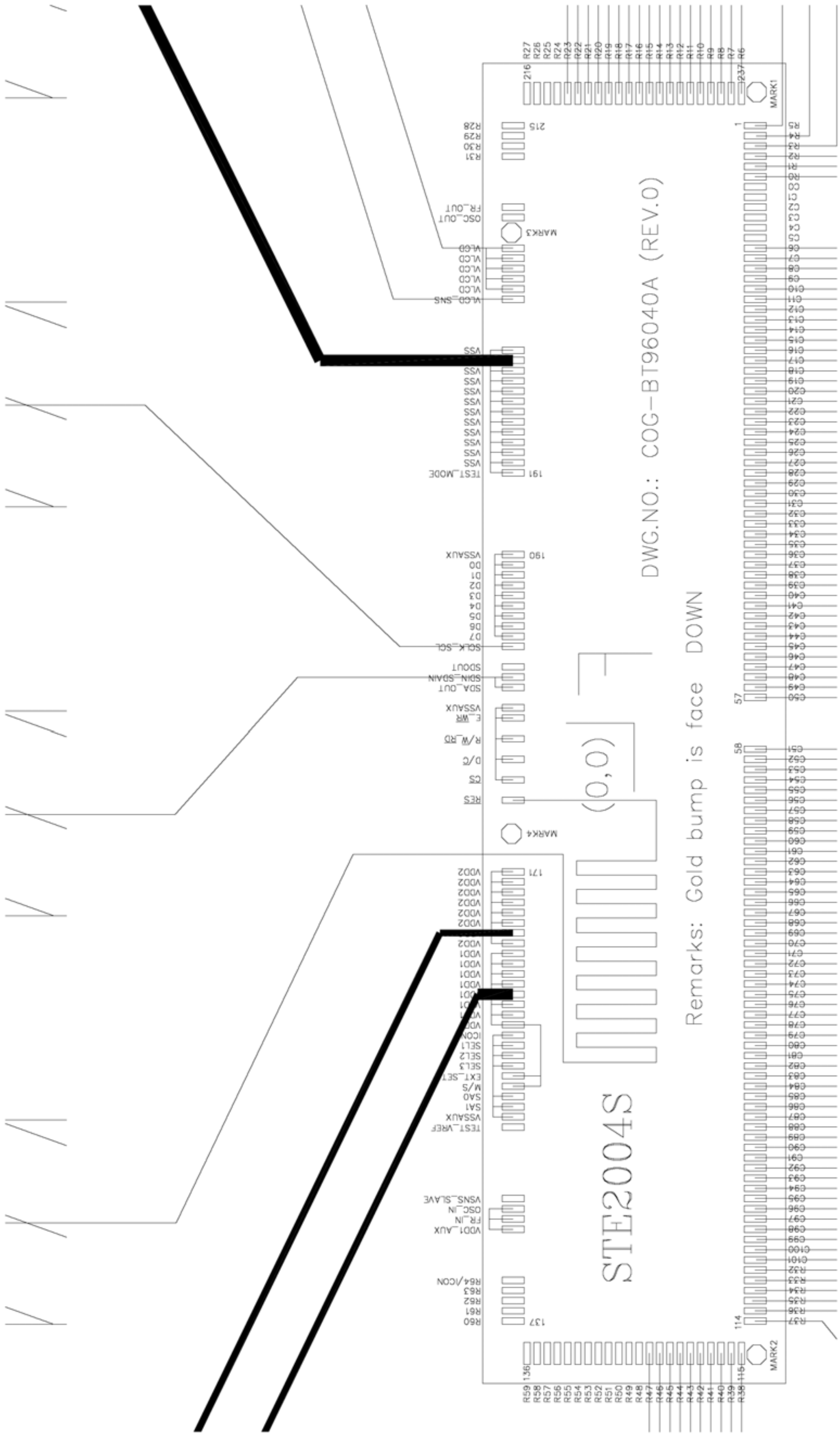



Figure 9: LCD drawing 5

DWG.NO.: COG-BT96040A (REV.1)

LCD I/O PIN

| PIN | DESCRIPTION |
| --- | --- |
| 1 | VDD |
| 2 | $\overline{RES}$ |
| 3 | SDA |
| 4 | SCL |
| 5 | VSS |
| 6 | VLCD |

Figure 10: LCD drawing 6

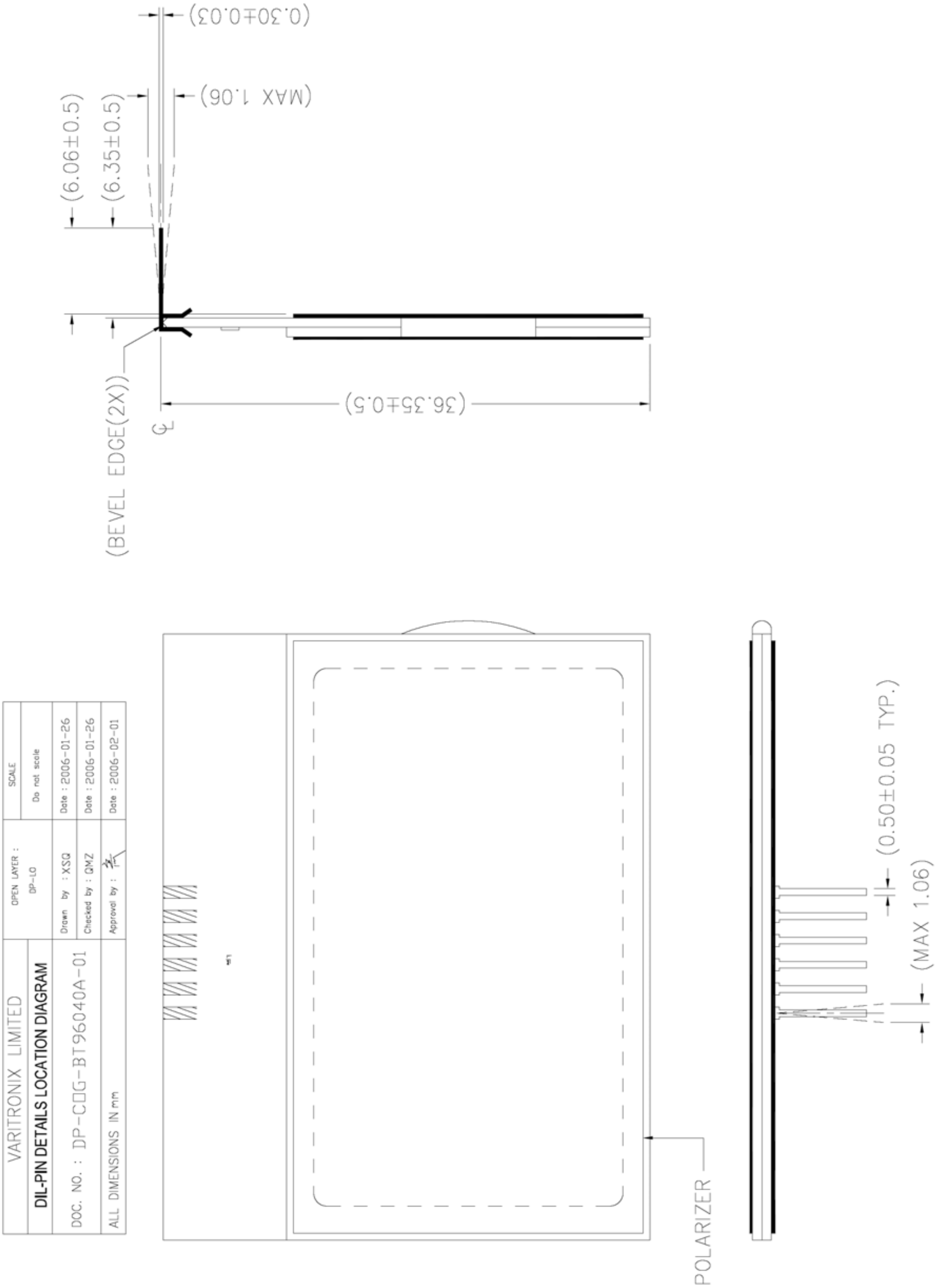



Figure 11: LCD drawing 7

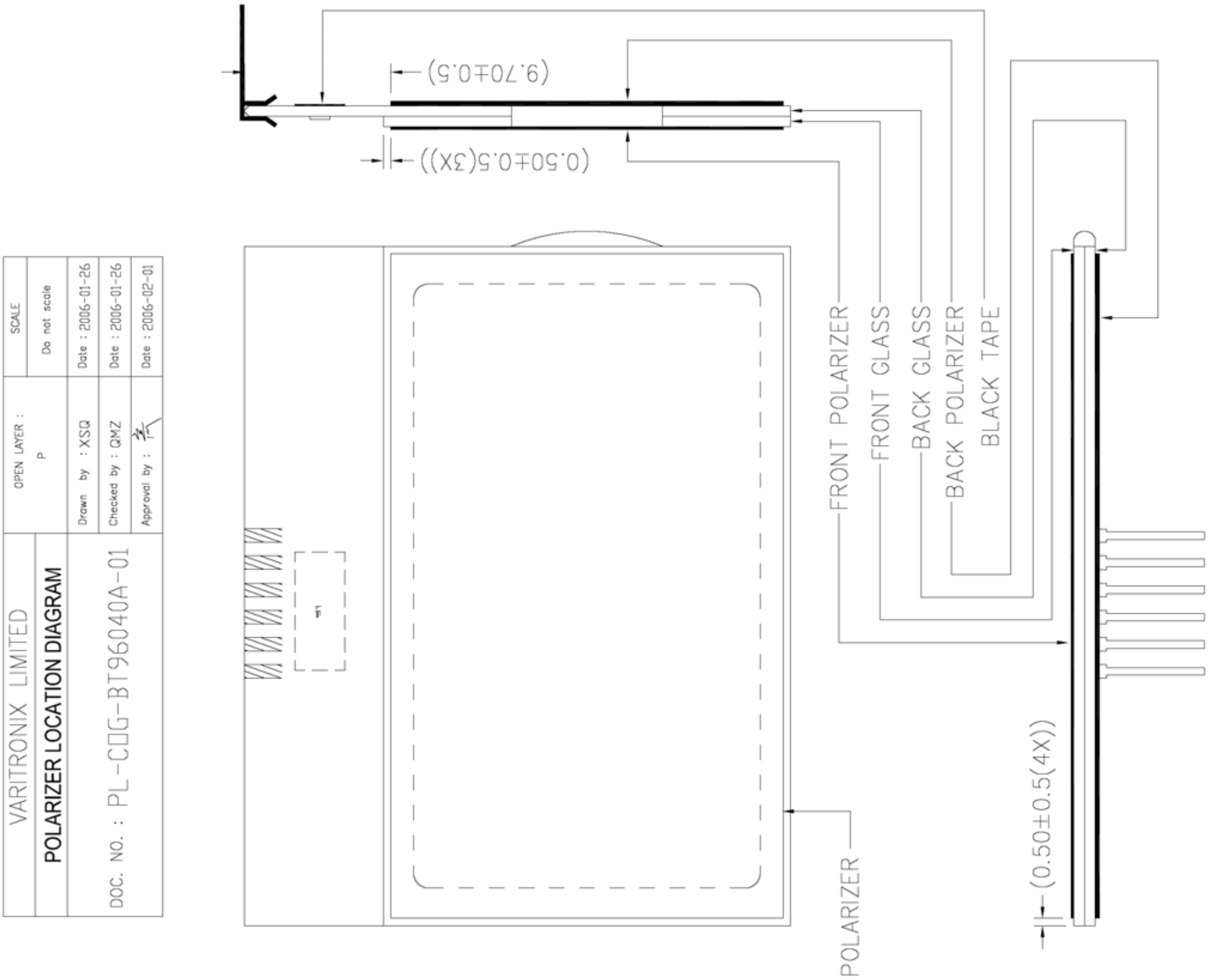



Figure 12: LCD drawing 8

**8. LCD Cosmetic Conditions**

a.) Reference document follow VL-QUA-012B.

b.) LCD size of the product is small.

- END -

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